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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,032	08/22/2003	Oliver Dieter Landolt	10011475-1	9255

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EXAMINER	
LUI, DONNA V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,032	LANDOLT, OLIVER DIETER	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5* is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 6-8* is/are allowed.

6)☒ Claim(s) *9,15-17, and 19-20* is/are rejected.

7)☒ Claim(s) *10-14 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim19 is objected to because of the following informalities: grammatical errors, examiner would like to suggest the following correction.

Claim 19, line 5: second reference current and current through a second current capacitively fedback from

Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 9, 15-17 and 19-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Itakura et al. (Pub. No.: US 2002/0180685 A1) in view of Ozawa (Pub. No.: US 2002/0000969 A1).

With respect to **Claim 9**, Itakura discloses a driving circuit *(See figure 31)*. Itakura teaches the driving circuit to comprise an output transistor *(Mp43)* connected between a voltage terminal *(Vdd)* and an output node *(node that is common to the resistor Rf and the terminals of Mp43 and Mn43)* to produce an output signal on the output node. Itakura teaches the output transistor to include a control terminal *(the control terminal is connected to a node common to*

Cf1, where the node connects to the terminal of Mp45); a current source *(Ib1)* connected to the control terminal of the output transistor to provide a reference current *(the connection of the current source to the control terminal of the output transistor is either through Mn41 when the switch SW20 is closed or through Mn42)*; a feedback capacitor *(Cf1)* connected from the output node to the control terminal of the output transistor to control a rate of signal change on the output node.

Itakura does not mention a memory connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal from a previous operating cycle in which the output transistor was activated.

Ozawa teaches a memory being configured to store a signal from the previous operating cycle *(See page 12, claim 6: second line memory; See figure 9, 330: second line memory)*.

Ozawa modifies the driving circuit of Itakura by inserting a second line memory at the node common to the gate of the output transistor *(Mp43)*, feedback capacitor *(Cf1)*, and switch *(Mn42)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a memory connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal from a previous operating cycle in which the output transistor was activated, as taught by Ozawa, to the driving circuit of Itakura, so as to generate a determination signal with a simple structure *([0018], last two lines; the determination signal is equivalent to the signal on the control terminal of the output transistor)*.

With respect to **Claim 15**, Itakura teaches a second output transistor *(Mn43)* connected between the output node *(node that is common to the resistor Rf and the terminals of Mn43 and Mp43)* and a second voltage terminal *(Vss)*, the second output transistor including a control terminal *(the control terminal is connected to a node common to Cf2, where the node connects to the terminal of Mn45)*; a second current source *(Ib2)* connected to the control terminal of the second output transistor to provide a second reference current *(the connection of the current source to the control terminal of the output transistor is either through Mp41 when the switch SW21 is closed or through Mp42)*; and a second feedback capacitor *(Cf2)* connected from the output node to the control terminal of the second output to control a second rate of signal change on the output node.

Itakura does not teach a second memory connected to the control terminal of the second output transistor, the second memory being configured to store a signal on the control terminal of the second output transistor from a previous operating cycle when the second output transistor was activated.

Ozawa teaches a memory being configured to store a signal from the previous operating cycle *(See page 12, claim 6: second line memory; See figure 9, 330: second line memory)*.

Ozawa modifies the driving circuit of Itakura by inserting a second line memory at the node common to the gate of the output transistor *(Mn43)*, feedback capacitor *(Cf2)*, and switch *(Mp42)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a second memory connected to the control terminal of the second output transistor, the second memory being configured to store a signal on the control terminal of

the second output transistor from a previous operating cycle when the second output transistor was activated, as taught by Ozawa, to the driving circuit of Itakura, so as to generate a determination signal with a simple structure *([0018], last two lines; the determination signal is equivalent to the signal on the control terminal of the output transistor).*

With respect to **Claim 16**, Itakura teaches a method for driving an electrical device, where the method comprises receiving an input signal *(See figure 31, input signal ~ IN- and IN+)*, outputting a signal in response to an input signal to produce an output signal on an output node *(node that is common to the resistor Rf and the terminals of Mp43 and Mn43)*, and controlling the output signal on the output node using a difference between a reference current *(Ib1 ~ reference current)* and current capacitively fed back from the output node *(the current is capacitively fed back from the output node though the capacitor Cf1).*

Itakura does not teach applying a stored signal to an output transistor in response to an input signal to produce an output signal on an output node.

Ozawa teaches a memory being configured to store a signal from the previous operating cycle in response to an input signal *(See page 12, claim 6: second line memory ~ stored signal; See figure 9, 330: second line memory, input signal ~ Din).*

Ozawa modifies the driving circuit of Itakura by inserting a second line memory at the node common to the gate of the output transistor *(Mp43)*, feedback capacitor *(Cf1)*, and switch *(Mn42)* resulting in a stored signal that is applied to an output transistor in response to an input signal to produce an output signal on an output node.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a memory that stores a signal that is applied to an output transistor in response to an input signal to produce an output signal on an output node, as taught by Ozawa, to the driving circuit of Itakura, so as to generate a determination signal with a simple structure *([0018], last two lines; the determination signal is equivalent to the signal on the control terminal of the output transistor).*

With respect to **Claim 17**, Itakura does not teach storing a control signal on the output transistor as a stored signal.

Ozawa teaches a memory being configured to store a signal from the previous operating cycle in response to an input signal *(See page 12, claim 6: second line memory ~ stored signal; See figure 9, 330: second line memory, input signal ~ Din).*

Ozawa modifies the driving circuit of Itakura by inserting a second line memory at the node common to the gate of the output transistor *(Mn43)*, feedback capacitor *(Cf2)*, and switch *(Mp42)* resulting in a stored signal that controls the output transistor.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a memory for storing a control signal on the output transistor as a stored signal, as taught by Ozawa, to the driving circuit of Itakura, so as to generate a determination signal with a simple structure *([0018], last two lines; the determination signal is equivalent to the signal on the control terminal of the output transistor).*

With respect to **Claim 19**, Itakura teaches signal to a second output transistor *(See figure 31, Mn43 ~ second output transistor)* in response to an input signal *(input signal ~ IN- and IN+)* to change the output signal on the output node; and controlling a second output signal on the output node *(See figure 31, node that is common to the resistor Rf and the terminals of Mn43 and Mp43)* using a difference between a second reference current *(Ib2 ~ second reference current)* and current through a second current capacitively fedback from the output node to the second output transistor *(the current is capacitively fed back from the output node though the capacitor Cf2)*.

Itakura does not teach applying a second stored signal to a second output transistor in response to an input signal to change the output signal on the output node.

Ozawa teaches a memory being configured to store a signal from the previous operating cycle in response to an input signal *(See page 12, claim 6: second line memory ~ stored signal; See figure 9, 330: second line memory, input signal ~ Din)*.

Ozawa modifies the driving circuit of Itakura by inserting a second line memory at the node common to the gate of the output transistor *(Mn43)*, feedback capacitor *(Cf2)*, and switch *(Mp42)* resulting in a stored signal that is applied to an output transistor in response to an input signal to produce an output signal on an output node.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a memory that applies a second stored signal to a second output transistor in response to an input signal to change the output signal on the output node, as taught by Ozawa, to the driving circuit of Itakura, so as to generate a determination signal with a simple

structure *([0018], last two lines; the determination signal is equivalent to the signal on the control terminal of the output transistor).*

With respect to **Claim 20**, Itakura teaches additional switches used in the electrical device where the switches alternately activate the first output transistor and the second output transistor *(See figure 33: modification of figure 31, [0123] and [0125], the additional switches allow for the alternate selection of the output transistors).* It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use additional switches such that the first and second output transistors are alternately activated, to a previous embodiment of Itakura, so as to enable the current at the output stage to be set easily *([0121]).*

Allowable Subject Matter

3. **Claims 1-4 and 6-8** are allowed.

With respect to **Claim 1**, none of the prior art teaches a current source being configured to generate a reference current proportional to a reference voltage and a reference frequency.

4. **Claims 10-14 and 18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to **Claim 10**, none of the prior art teaches a memory which includes a memory capacitor and an amplifier, the amplifier being connected to the memory capacitor and the output transistor such that the amplifier is selectively configured in a voltage follower configuration to store the signal on the control terminal of the output transistor in the memory capacitor.

With respect to **Claim 12**, none of the prior art teaches a current source being configured to generate a reference current proportional to a reference voltage and a reference frequency.

With respect to **Claim 18**, none of the prior art teaches the controlling includes generating a reference current using a reference frequency and a reference voltage, and applying the reference current to a control terminal of the output transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donna V Lui
Examiner
Art Unit 2629

AMR A. AWAD
PRIMARY EXAMINER